

***Amendments to the Drawings***

Attached hereto are 33 replacement sheets of formal drawings for FIGS. 1-6, 7A-C, 8A-D, 9-10, 11A-C, 12A-B, 13A-B, 14-16, and 17A-H, corresponding to the informal sheets of drawings originally filed with the application.

The attached sheet of drawings for FIG. 10 includes changes. FIG. 10 has been amended to change three reference numbers in order to make FIG. 10 consistent with the description on page 21, lines 12-13 of the specification. An annotated sheet showing the changes to FIG. 10 is attached.

***Remarks***

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 25-34 are pending in the application, with 25, 26, 27 and 29 being the independent claims. Claim 25-30 are sought to be amended to further clarify the invention. New claims 31-34 are sought to be added. The title has been amended to read "High Performance RISC Instruction Set Digital Signal Processor Having Circular Buffer and Looping Controls". FIG. 10 and the paragraph starting on page 10, line 1 of the specification have been amended to correct minor informalities. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

***Rejections under 35 U.S.C. § 102***

On page 3 of the Office Action, claims 25-30 were rejected under 35 U.S.C. §102(b) for allegedly being anticipated by U.S. Patent No. 5,717,947 to Gallup *et al.* ("Gallup"). Applicants respectfully traverse this rejection.

As described in the present application, DSP algorithms (e.g., filters) organize data into circular buffers. (*See* page 20, lines 16-17 of the present application.) In an embodiment of the present invention, circular buffer control logic compares a circular buffer pointer to an address stored in a circular buffer end register. If the pointer matches the address, an address stored in an associated circular buffer start register is

restored to the register file. (*See* page 21, lines 16-18 of the present application.) The circular buffer control logic facilitates working with different data widths. (*See, e.g.,* page 21, lines 8-10 of the present application.) Accordingly, claim 25 recites:

25. A circular buffer control circuit, comprising  
a first number of circular buffer start registers;  
a first number of circular buffer end registers, each  
associated with a different one of the circular buffer start  
registers; and  
circular buffer control logic including  
means for comparing a pointer to a first  
address stored in a selected one of the circular buffer end  
registers, and  
means for restoring to a register file a  
second address stored in the one of the circular buffer start  
registers associated with the selected circular buffer end  
register, if the pointer matches the first address stored in the  
selected circular buffer end register.

Similar features are recited in claim 26.

The combination of features recited in claims 25 and 26 are neither taught nor suggested by Gallup. For example, the Examiner applies column 45, lines 46-48 of Gallup for teaching the claimed "means for restoring". According to Gallup:

The Repeat Begin Register (RBR) 180 is used by the repeat and repeate instructions to allow rapid execution of the inner loop of programs. The RBR is illustrated in more detail in FIG. 2-55. When the repeat or repeate instruction is executed, a value of PC+2 is loaded into the RBR. At the end of the loop (when the value in the Repeat End Register (RER) matches the address of the instruction currently being executed), the Program Counter (PC) is loaded with the contents of the RBR.

*See* Gallup at column 45, lines 46-54. As illustrated by this passage, Gallup relates to instructions rather than data and loads the instruction address stored in the RBR into the program counter. This is not equivalent to "means for restoring to a register file a second

address stored in the one of the circular buffer start registers associated with the selected circular buffer end register" as recited, for example, in claim 25 of the present application. Thus, for at least this reason, claim 25 is patentable over Gallup. Claim 26 recites a similar feature and is also patentable over Gallup.

Claim 27 of the present application recites:

27. A digital signal processor, comprising:  
a register set; and  
means for executing a loop of instructions a specified number of times determined by a loop count value, including  
first means for executing a first instruction specified by address bits stored in a first portion of a first register of the register set,  
second means for decrementing the loop count value stored in a second register of the register set, and  
third means for executing a second instruction specified by address bits stored in a second portion of the first register and a third register of the register set.

Similar features are recited in claim 29.

The combination of features recited in claims 27 and 29 are neither taught nor suggested by Gallup. For example, nowhere does Gallup teach or suggest, for example, the feature of "third means for executing a second instruction specified by address bits stored in a second portion of the first register and a third register of the register set" as recited in claim 27. Thus, for at least this reason, claim 27 is patentable over Gallup. Claim 29 recites a similar feature and is also patentable over Gallup. Claims 28 and 30 depend from independent claims 27 and 29 respectively, and are patentable over Gallup for at least the same reasons as claims 27 and 29 and further in view of their own respective features.

Reconsideration and withdrawal of the rejection of claims 25-30 are respectfully requested.

***New Claims 31-34***

Applicants have added new claims 31-34 to further clarify the invention. Support for new claims 31 and 33 is found, for example, on page 21, lines 1-2. Support for new claims 32 and 34 is found, for example, in FIG. 11A.

Claims 31-34 depend from one of independent claims 25 and 26, either directly or indirectly, and are patentable over Gallup for at least the same reasons as claims 25 and 26 and further in view of their own respective features. It is believed that these claims can be examined without conducting a new search.

Consideration and allowance of new claims 31-34 are respectfully requested.

***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read "Virgil L. Beaton". The signature is fluid and cursive, with a large, stylized initial "V".

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Date: April 10, 2006

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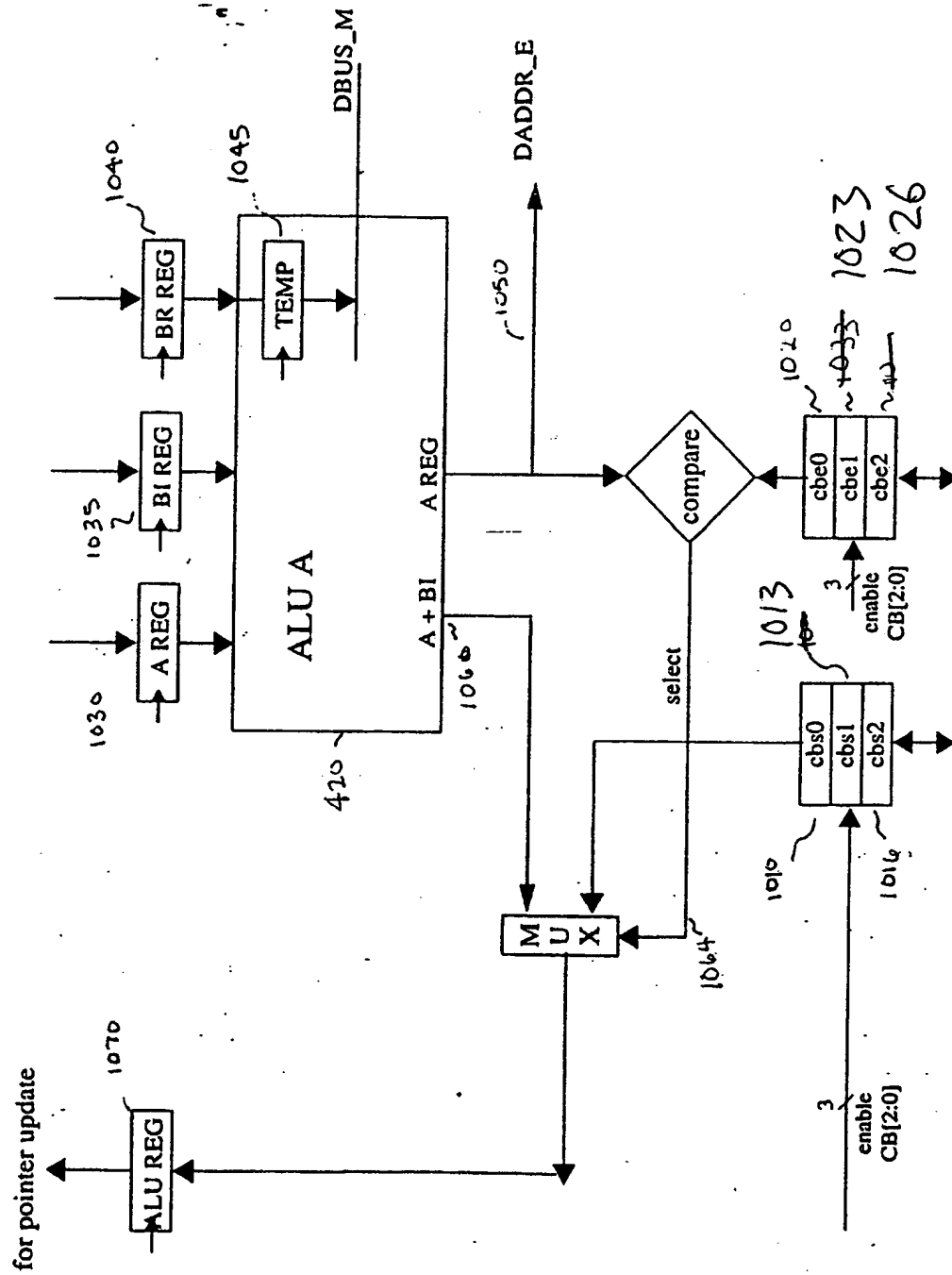


FIG. 10